ATCA Carrier Board
with Dedicated IPMI Controller (2)

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Outline

- Hardware structure of IPMC
- IPMC Software
- Summary
Structure of Renesas-based IPMC

- AMC BAY 1
- AMC BAY 2
- AMC BAY 3
- Sensors
  - MAX16031 Temp., Volt., Curr.
  - MAX6626 Temperature1
  - MAX6626 Temperature2
  - ATC210 DC/DC Temp., Volt., Curr.
- Peripherals
  - AT24C512 EEPROM
  - Peripheral I2C

- Front Panel
  - Hot-swap plug
  - Blue LED

- IPMB-0-A
- IPMB-0-B

- Zone 1
I2C connections

- Intelligent Platform Management Bus (IPMB–0)
  - 2 redundant channels
- Intelligent Platform Management Bus (IPMB–L)
  - Separate channels for AMC Modules
- Peripheral bus
Software

- Initialization part
  - Control register configuration
  - Peripheral configuration

- Main Loop
  - Event processing
  - IPMB-0 messages handling
  - IPMB-L messages handling
Event handling

- **Problem:**
  - Low response times to various events are essential for LLRF control system
  - Long ISR execution time = missing other events

- **Solution:**
  - Event-driven cyclic executives solution in conjunction with external device interrupts
  - ISRs only feed the main event handling loop (if possible)
Message queuing

- **IPMB–0**
  - Single incoming queue
  - Single outgoing queue
  - Round robin algorithm

- **IPMB–L**
  - Single incoming queue
  - Separate outgoing queues
Summary

- Greater clock frequency speeds up the operation of the device
- Six I2C channels provide stable and parallel communication with all the components on the IPMB
- Single-device IPMC
  - Increases the reliability
  - Facilitates the software development and maintenance
  - Removes the need for interfacing between devices
THE END

- Questions?
- Comments?