ATCA Carrier Board
with Dedicated IPMI Controller (1)

P. Perek, D. Makowski, P. Predki, A. Napieralski
Technical University of Lodz
Department of Microelectronics and Computer Science
Lodz, Poland

We acknowledge funding from the European Commission under the FP7 Research Infrastructures project EuCARD, grant agreement no. 227579.
Outline

- ATCA-based LLRF Control System of XFEL
- Intelligent Platform Management Controller
- Previous and current IPMC solutions
- Summary
LLRF Control System of XFEL

- Tasks of LLRF system of XFEL accelerator:
  - Control of the cavity resonance frequency,
  - Data acquisition,
  - High-frequency signal processing.

- This system requires stable continuous operation.

- It was decided to build the prototype system based on ATCA specification.
ATCA standard

- ATCA standard ensures high level of:
  - Reliability,
  - Availability,
  - Serviceability.
- Modular design allows flexible configuration.
- Hot Swap mechanism allows modules exchange during normal system operation.
- Providing all these functionalities is possible thanks to use of a complex IPMI management system.
Intelligent Platform Management in ATCA shelf

External System Manager

Shelf Manager (Backup)
- IPMC

Shelf Manager (Active)
- IPMC

Power Entry Module
- IPMC
- Fan Set

Power Entry Module

IPMB-0

IPMB-1

ATCA Carrier Board
- MMC AMC
- MMC AMC
- MMC AMC

ATCA Board

IPMC

ATCA Board

IPMC

2x Redundant Radial IP-Capable Transport
The Role of IPMC

- Control of hot-swap activation and deactivation,
- Management of on-board sensors,
- Early detection of faults – event generation,
- Electronic Keying management,
- Supervision of Advanced Mezzanine Cards.
Previous solutions of IPMC

- IPMC consists of two devices:
  - Atmel Atmega1281
  - Xilinx Spartan 3

- Faults of microcontroller:
  - Only one built-in I2C interface
  - Small number of I/O pins
  - Low frequency of CPU operation
  - Small amount of RAM
Renesas H8S/2166

- Microcontroller dedicated for management systems in telecommunication applications
- Essential features:
  - 16-bit CPU operating at a frequency of 32 MHz
  - ROM: 512 kbytes, RAM: 40kbytes
  - Six-channel I2C bus interface
  - General I/O pins: 106
- Meets all the requirements
Summary

- Greater clock frequency speeds up the operation of the device
- Six I2C channels provide stable and parallel communication with all the components on the IPMB
- Single-device IPMC
  - Increases the reliability
  - Facilitates the software development and maintenance
  - Removes the need for interfacing between devices
THE END

- Questions?
- Comments?