AMC Timing Receiver and Clock Synthesizer Module for the LLRF System

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Abstract—**The new LLRF system architecture based on the ATCA platform was developed and tested at FLASH. The LLRF system require generation of highly stable clock and trigger signals for system operation and initiation of timing events. This paper describes the conception, design and performance test results of the AMC module designed to fulfill the LLRF system synchronization needs. This module contains three independent clock synthesizers that are able to generate LVDS clock signals in the range 10 MHz to 100 MHz. These signals are put to the AMC connector and can be distributed over the entire ATCA crate. The clock synthesizers can be synchronized either by an internal quartz oscillator or an external 1.3 GHz reference signal provided to the board either via the AMC connector or via a front panel junction. This assures flexibility when using the board for tests and for the LLRF system operation. Besides clock synthesizers the AMC card contains an optical receiver suited to convert and decode FLASH timing signals distributed in the FLASH accelerator system.**

Index Terms—**Timing; clock; AMC; synthesizer; jitter**

I. Introduction

The modern superconducting linear accelerator facilities such as the European XFEL use highly stable RF field for the acceleration of the electron beam. The field stabilization is performed by the LLRF system [1] including high performance RF and digital subsystems. The LLRF system must support acquisition and processing of more than 100 high frequency (1.3 GHz) measurement signals at each RF station of the accelerator. The scale of the LLRF control system, the data transfer rates, the number of implemented software applications, the required performance and finally, the required high availability and modularity lead to a decision that the xTCA[1] standard [2] will be used as the main hardware platform for the XFEL accelerator.

The xTCA based LLRf system has been designed and the first prototype performance was evaluated at the FLASH accelerator [3]. Amongst multiple requirements fulfilled by the system architecture there are the modularity and high reliability. These requirements imply using modules of specified functionality. Minimum two modules of given type could be installed in one operating system in order to provide redundancy and thus, together with the intelligent ATCA platform management system, fulfill the high reliability requirements.

Most of the specified modules, like the ADC cards, CPU's and vector modulators require synchronization with another devices and with the measured RF signals. The overall RF stations synchronization in the entire accelerator is performed by the RF phase reference and timing distribution system [4].

In general, there are two types of synchronization signals: the phase reference (from the Master Oscillator - MO) and the timing signals. The MO signal is an analog (harmonic) highly phase stable signal and is distributed by coaxial cables or analog optical fiber links. The phase reference signal is used as a input for analog subcomponents of the LLRF system (like vector modulator) and for generation of synchronous low jitter clock signals for the digital part of the system. The timing signal is a digital, coded signal carrying the information about triggers and various accelerator states like event codes and unique numbers for identification of e.g. pulse or electron bunch numbers.

Both the MO and the timing signals, provided to the xTCA crate should be split and distributed internally to all relevant devices. For this purpose an AMC timing receiver and clock synthesizer module (called further in this text the AMC-TM) was designed. The design and performance of the AMC-TM card is described in the remnant of this paper.

II. ATCA Based LLRF System Hardware Architecture

The ATCA based LLRF system is using a three-slot ATCA carrier board [5]. It was assumed that an AMC module of any functionality can be operated in any of the slots available in the ATCA crate. Therefore there is a flexibility in using of the AMC-TM. Furthermore, there can be two AMC-TM modules in one crate and in case of failure of one of them, the other, functioning module can take over the generation of timing signals.

The conceptual hardware layout for the timing signal distribution is shown in Fig. 1. The AMC-TM localized in one of the AMC bays of the ATCA carrier generates clock and trigger signals. Those signals are distributed to the remaining

1 The "X" stands either for "μ" or for "A"- respectively μTCA and ATCA

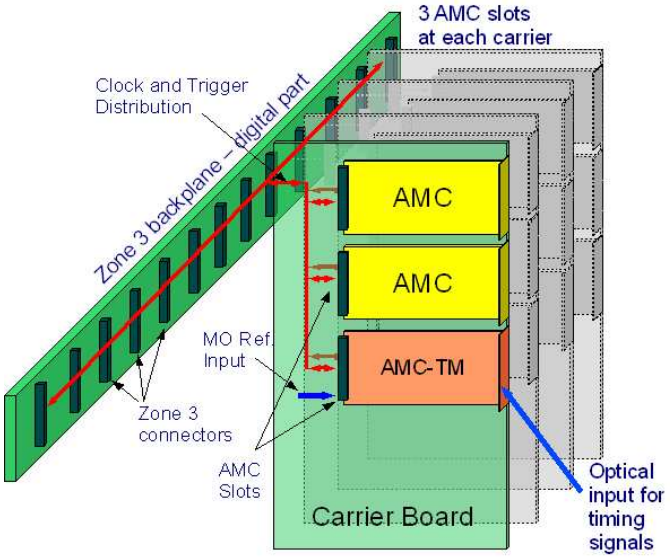

Figure 1. The ATCA based LLRF system hardware conception with exemplary AMC-TM location and clock distribution scheme.

AMC slots on the carrier board and over a custom Zone 3 Backplane to all other carrier boards present in the system. The hardware allows for bi-directional signal distribution, therefore the AMC-TM can be localized in any AMC slot at any carrier board in the crate.

Due to various types of modules that can be installed in the system, the AMC-TM should generate 3 independent clock and 3 trigger signals. All these signals are distributed over the entire ATCA crate as shown in Fig. 1. The required maximum clock jitter value is 5 ps. The trigger signal jitter value is of low importance because the triggered events are of relatively low frequency.

The LLRF system conception assumes installing a full-size AMC modules composed of two Printed Circuit Boards (PCBs): the top module (AMC-B) [6] and the bottom module (AMC-A). The top module is an universal PCB containing all hardware components necessary for communications with the ATCA systems and specified digital I/O for controlling of the bottom module. The AMC-A can contain custom electronics (also analog) realizing given functionality for the system, e.g. the vector modulator. The top and bottom modules are connected by universal connector used for transmission of differential signals and power supplies. One of the functional AMC-A modules is the AMC-TM board being the subject of this paper.

III. Prototype Board Conception

The conceptual block diagram of the AMC-TM module is shown in Fig. 2. Both AMC-A and AMC-B PCBs are shown. The AMC-A construction is described in the following sections of this paper.

Two independent hardware parts can be distinguished in the AMC-TM hardware. The clock synthesizer circuits and the timing signal receiver.

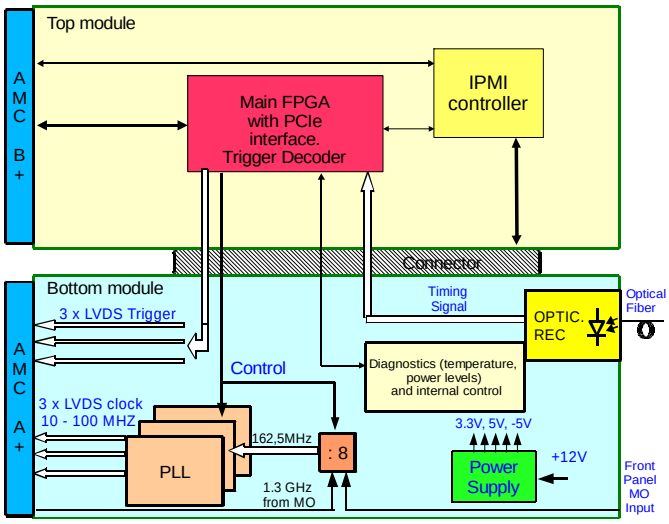

Figure 2. The block diagram of the AMC-TM module.

The MO phase reference signal can be provided either by the the AMC-A+ edge connector or by a front panel connector. After frequency division the signal is provided to three independently controlled frequency synthesizers that can output LVDS clock signals in frequency range of 10 MHz to 100 MHz. All synthesizers are controlled by the AMC-B module.

The timing signal receiver uses an optical receiver compatible with the FLASH accelerator timing system optical fiber connectors. Obtained electrical signal is transmitted to the AMC-B card, where trigger decoding algorithms are implemented in the FPGA. Generated trigger signals are sent back to the AMC-A module and provided to the AMC edge connector.

The AMC-TM board contains also diagnostic and microcontroller circuits. The diagnostic circuits monitor the temperature of the board, the availability of input signals, the board component status (like PLL lock) and the values of power supply voltage. The diagnostic information can be read out by the AMC-B card and used by the crate management software for fault detection and for switching between the redundant units.

The microcontroller circuit allows for the synthesizer part configuration without the use of the AMC-B module. The purpose of this option is to test the board performance in laboratory conditions without the complex top module. The results could give the information about the clock signal degradation by the AMC-B part operation when compared with the laboratory tests outside the ATCA crate.

IV. Clock Synthesizer Circuit

The block diagram of one PLL clock synthesizer channel is shown in Fig. 3. The input frequency divider can use signal provided either from the AMC edge connector or from the front panel of the AMC module. Additionally a highly stable on board crystal oscillator circuit can provide a reference clock

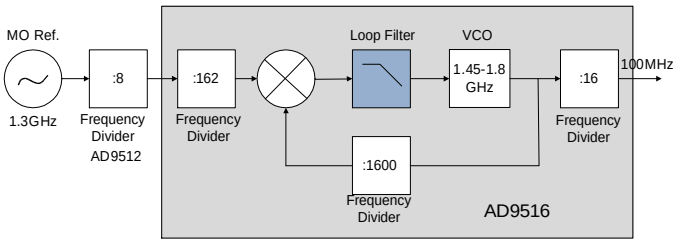

Figure 3. Block diagram of the clock signal synthesizer (one channel).

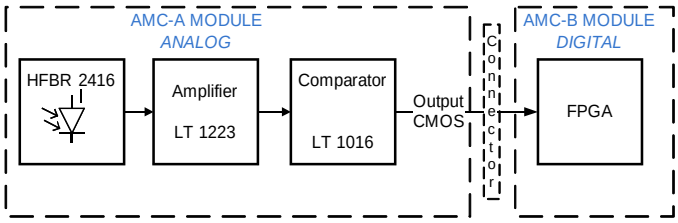

Figure 4. Block diagram of the timing signal receiver part.

in case when the MO signal is missing or when the ATCA crate is tested in laboratory independently from the accelerator control system.

Frequency divider chip with fanout and differential output was selected to be able to drive three clock synthesizer chips simultaneously. The MO signal frequency is divided to a value acceptable for the the PLL synthesizer input (below 250MHz). The complex synthesizer chip architecture with internal 1.6 GHz VCO allows for very broad range of configurations and very flexible selection of the output frequency value. Example divider settings for 100 MHz clock frequency are shown in Fig. 3. The required clock frequency range is 10 MHz to 100 MHz with 1 MHz step but designed architecture allows for generation of signals in much broader frequency range with fine resolution and also fractional ratios to the input frequency value. The synthesizer circuit allows also for phase adjustments of the clock signals.

The LVDS output signals of the clock synthesizer chips are fed over the AMC connector to the ATCA carrier board for further distribution. Advanced design techniques for low-jitter signals propagation were applied in order to minimize the degradation of the signal performance.

V. Timing Receiver Details

The timing signal receiver block diagram is shown in Fig. 4. The optical receiver module converts the signal received by the optical fiber to electrical signal which is amplified and provided to a comparator circuit. The latter one forms a CMOS compatible signal which is sent to the FPGA for decoding. As described above, the decoded trigger signals are transmitted back to the AMC-A and further to the ATCA carrier board. The algorithm implemented in the FPGA can decode up to three different event triggers. The CMOS standard was selected due to much simpler requirements for board routing than for the differential signals and the electrical performance is still sufficient.

VI. PCB Design

An eight-layer PCB was designed for the AMC-TM card. Signal integrity techniques were applied in order to assure the high clock signal performance. Low loss and improved quality substrate was selected for the circuit. Precise track routing and differential pair equalization were performed in the areas where clock signals are distributed. The RF transmission line routing, impedance matching and RF grounding techniques were used for distribution of the 1.3 GHz MO signal. Complex power supply network was used with separate low noise voltage regulators supplying each sensitive device on the board. By this a good isolation between board sub-circuits and also interference suppression from the digital AMC-B was achieved.

Multiple test points and configuration components were foreseen in the board in order to make possible extensive tests of the board performance in laboratory conditions. The pictures of designed device are shown in Fig. 5. More detailed description of the conception and the hardware design can be found in [7].

VII. Performance Tests

Extensive laboratory tests have been performed on the clock synthesizer circuits [7]. As it was described in the section IV, there is very large flexibility in setting up of the output frequency value of the PLL synthesizer. Unfortunately, the clock jitter value strongly depends on the frequency of the signals provided to inputs of the PLL phase detector (so called comparison frequency). In general the higher the frequency, the higher the jitter performance. Furthermore, the jitter value, at given comparison frequency depends also on the loop filter parameters and on the output frequency value. The AMC-TM architecture allows for fixing the comparison frequency value and still fulfilling the tuning range and step requirements. By this the loop filter bandwidth can be fixed and divider settings determined for the best clock signal performance. This requires significant complexity of the synthesizer control software.

Simulations were performed where various comparison frequency values were investigated along with the loop filter parameters in order to find relationships between jitter values and synthesizer settings. It was found that there is an optimum loop bandwidth for given comparison frequency. The simulations results were confirmed by measurements performed in laboratory conditions. The Signal Source Analyzer device was used for clock jitter measurements.

Measurement results for the comparison frequency value of 1 MHz are shown in Table 1. The jitter values of over 7 ps were measured for the loop bandwidth of 5 kHz. For 16 kHz, there is optimum, excellent jitter values even below 1 ps!. When increasing the loop bandwidth, the jitter values increase again.

The example measurement screen-shot is shown in Fig. 6. These measurements were performed in the laboratory at the outputs of the AMC-TM board. Results of 1 ps clock jitter fulfill the design requirements for the board. But the jitter can be significantly affected by the distribution within the ATCA carrier board and over the Zone 3 Backplane.

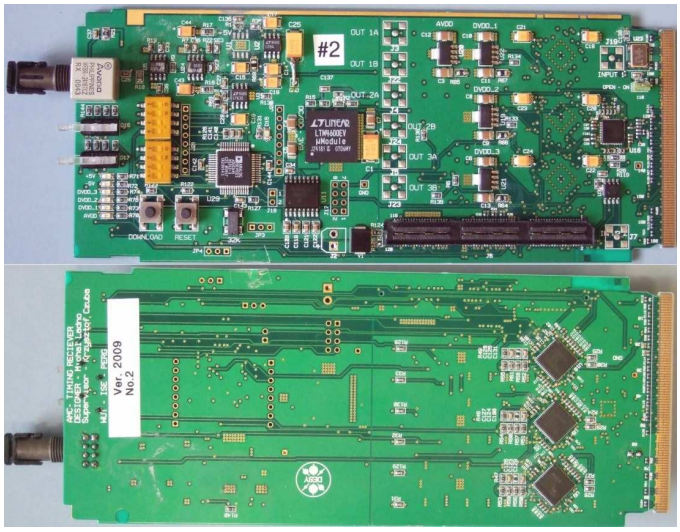

Figure 5. The assembled AMC-TM card.

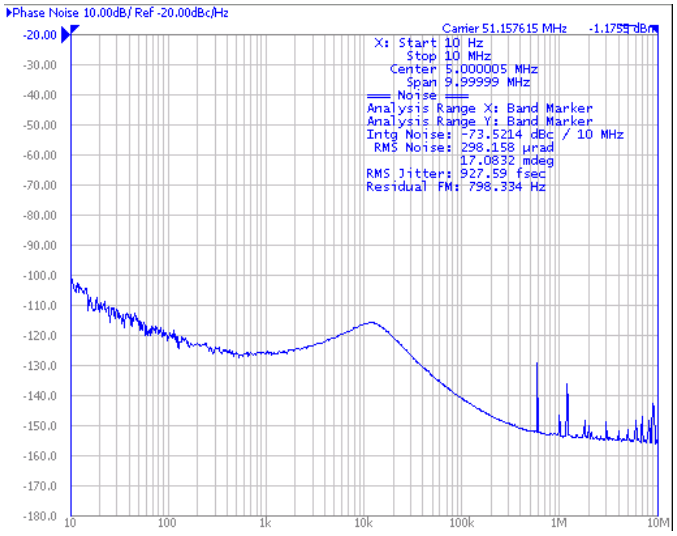

Figure 6. Clock jitter measurement example.

TABLE I. THE MEASURED PHASE JITTER VALUES IN PS FOR THE COMPARISON FREQUENCY OF 1MHZ

Loop Filer Bandwidth [kHz]	**Clock Frequency**		
	20 MHz	***51 MHz***	***99 MHz***
5	7,07	7,11	7,33
16	**1,32**	**0,93**	**0,97**
100	1,77	1,59	1,64

This is an issue exceeding the scope of this paper but such tests are planned.

VIII. SUMMARY

The conception and design of the AMC clock synthesizer and timing receiver board is described. The eight-layer PCB provides the possibility of synthesizing three low jitter independently programmable clock signals. It also allows for receiving and decoding of the optical trigger signals from the FLASH accelerator timing system. Together with the AMC-B module, the designed board allows for fulfilling the timing requirements of the ATCA based LLRF system. The system availability is supported by extended diagnostic capabilities implemented in the board where the system components state, the availability of input signals and the board temperature can be read out and sent to the ATCA management software. The measured excellent clock jitter values show that the design and board configuration was performed correctly. Further plans foresee extensive performance tests of the board installed in the operating ATCA system.

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REFERENCES

[1] S. Simrock et al. Digital low-level rf controls for future superconducting linear colliders. PAC05, pages 515–519.

[2] S.N. Simrock, V. Ayvazyan, A. Brandt, M. Hüning, W. Koprek, F. Ludwig, P. Pucyk, K. Rehlich, E. Vogel, H.C. Weddig, M. Grecki, T. Jezynski, W. Jalmuzna. Conceptual llrf design for the european xfel – LINAC 2006, Knoxwille, Tennessee, USA.

[3] Evaluation of an ATCA Based LLRF System at FLASH, S. Simrock, M. Grecki, T. Jeżyński, W. Koprek, Ł. Butkowski, G. Jabłoński, W. Jałmużna, D. Makowski, A. K. Czuba, Proc. 16th Int. Conf. Mixed Design of ICs and Systems, Lodz, 25-27 June 2009

[4] K. Czuba, K Antoszkiewicz, S. Simrock, H. Weddig, “The RF Phase Reference Distribution System for The European XFEL”, PAC09, Vancouver, Canada, May 2009.

[5] T. Jezynski et al, “Prototype AdvancedTCA Carrier Board with three AMC bays”, Nuclear Science Symposium Conference Record, 2008. NSS '08.

[6] D. Makowski and A. Piotrowski and A. Napieralski , “Universal communication module based on AMC standard,” Mixed Design of Integrated Circuits and Systems (MIXDES) 2008, Pozna, Polska, 2008.

[7] M. Ladno, “AMC timing receiver and clock synthesizer module for the LLRF system”, Msc Thesis, Warsaw University of Technology, Poland, 2008.